CLAIMS:

1. A method for changing over a serially networked system (100), in particular a serial databus system, from subnetwork operation (T), in which at least one node (22, 28) and/or at least one user (32, 38) of the system (100) is in a state of reduced current consumption and is not addressed and/or not activated by the signal level (40, 42, 44) of the data traffic on the system (100), to full network operation (G), in which all the nodes (20, 22, 24, 26, 28) and/or all the users (30, 32, 34, 36, 38) of the system (100) are addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the system (100) is changed over from subnetwork operation (T) to full network operation (G) if a signal rest level (50) and/or no change in the signal level is noted on the system (100) for a period (Δt) which is greater than a critical period (Δt_k) of definable or settable length.

2. A method as claimed in claim 1, characterized in that the critical period (Δt_k) is selected to be greater than the interval (Δt_d) between the individual messages or data packets of the data traffic on the system (100).

3. A method as claimed in claim 1 or 2, characterized in that messages or data packets are sent by at least one of the nodes (20, 24, 26) and/or users (30, 34, 36) participating in subnetwork operation (T) at cyclic intervals which are smaller than the critical period (Δt_k).

4. A serially networked system (100), which is intended to be changed over from subnetwork operation (T), in which at least one node (22, 28) and/or at least one user (32, 38) of the system (100) is in a state of reduced current consumption and cannot be addressed and/or activated by the signal level (40, 42, 44) of the data traffic on the system (100), to full network operation (G), in which all the nodes (20, 22, 24, 26, 28) and/or all the users (30, 32, 34, 36, 38) of the system (100) may be addressed and/or activated by the signal level (46, 48) of the data traffic on the system (100), characterized in that the changeover from subnetwork operation (T) to full network operation (G) takes place if the system (100) is in the signal rest

level (50) state and/or an unchanged signal level state for a period (Δt) which is greater than a critical period (Δt_k) of definable or settable length.

5. A system as claimed in claim 4, characterized in that the critical period (Δt_k) is greater than the interval (Δt_d) between the individual messages or data packets of the data traffic on the system (100).

6. A system as claimed in claim 4 or 5, characterized in that at least one of the nodes (20, 24, 26) and/or users (30, 34, 36) participating in subnetwork operation (T) sends messages or data packets at cyclic intervals which are smaller than the critical period (Δt_k).

7. A system as claimed in at least one of claims 4 to 6, characterized in that the system (100) comprises at least one serial databus (10), in particular at least one C[ontroller]A[rea]N[etwork] bus.

8. A system as claimed in at least one of claims 4 to 7, characterized in that the user (30, 32, 34, 36, 38) takes the form of

- at least one system chip unit (80), in particular at least one system chip unit,
- and/or at least one microcontroller (90) unit provided for carrying out at least one application.

9. A transceiver unit (84), in particular for carrying out a method as claimed in at least one of claims 1 to 3 and/or in particular associated with at least one system (100) as claimed in at least one of claims 4 to 8, characterized in that the transceiver unit (84)

- is connected to at least one serial databus (10), in particular to at least one C[ontroller]A[rea]N[etwork] bus, and
- is in communication (982) with at least one microcontroller unit (90) which is provided to carry out at least one application.

10. A transceiver unit as claimed in claim 9, characterized by at least one control logic associated with the transceiver unit (84) and/or implemented in the transceiver unit (84).

11. A voltage regulator (86) which is connected to at least one battery unit (70), and which is in communication (886) with at least one transceiver unit (84), in particular as claimed in claim 9 or 10, which voltage regulator is intended to supply a voltage to at least one microcontroller unit (90), provided to execute at least one application, in the event of detection, by the transceiver unit (84), of at least one defined, in particular continuous and/or in particular symmetrical signal level pattern in at least one incoming message associated with at least one application and occurring on at least one serial databus (10), in particular on at least one C[ontroller]A[rea]N[etwork] bus.

12. A chip unit (80), in particular a system chip unit, for addressing and/or activating at least one microcontroller unit (90) which is provided to carry out at least one application and which is associated with at least one serial databus (10), in particular at least one C[ontroller]A[rea]N[etwork] bus; characterized by

- at least one transceiver unit (84) as claimed in claim 9 or 10, and
- at least one voltage regulator (86) as claimed in claim 11.

13. A microcontroller unit (90) provided to carry out at least one application and associated with at least one serial data bus (10), in particular at least one C[ontroller]A[rea]N[etwork] bus, which microcontroller unit is to be supplied with a voltage only if at least one defined, in particular continuous and/or in particular symmetrical signal level pattern is detected in at least one incoming message associated with at least one application and occurring on the databus (10), by at least one transceiver unit (84), in particular as claimed in claim 9 or 10.

14. A microcontroller unit (90) as claimed in claim 13, characterized in that the microcontroller unit (90) may be activated by the transceiver unit (84).

15. The use of

- a method as claimed in at least one of claims 1 to 3 and/or
- at least one system (100) as claimed in at least one of claims 4 to 8 and/or
- at least one chip unit (80) as claimed in claim 12 and/or
- at least one microcontroller unit (90) as claimed in claim 13 or 14 in

automobile electronics, in particular in motor vehicle electronics.